IN THE CLAIMS

Please amend claims 2 and 9 as indicated below.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (original) A method for maintaining synchronization in a home network that includes a host Ethernet media controller and an HPNA chip, where control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the method comprising the steps of:

(a) sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame; and

(b) recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs.

Claim 2 (currently amended) ~~The method of claim 1~~ A method for maintaining synchronization in a home network that includes a host Ethernet media controller and an HPNA chip, where control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the method comprising the steps of:

(a) sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame; and

(b) recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs;

wherein the null frame includes a source address field and an Ethernet type field, step (a) further including the step of providing an invalid address in the source address field and the Ethernet type field.

Claim 3 (original) The method of claim 2 wherein step (a) further includes the step of providing all-zeros in the source address field and the Ethernet type field.

Claim 4 (original) The method of claim 2 wherein step (a) further includes the step of providing the null frame as a minimum size Ethernet frame.

Claim 5 (original) The method of claim 2 wherein step (a) further includes the step of issuing from the host Ethernet MAC a minimum size frame containing a frame control word prior to the data frame during a transmit sequence.

Claim 6 (original) The method of claim 2 wherein step (a) further includes the step of issuing from the HPNA chip a minimum size frame containing a frame status word with the data frame during a receive sequence.

Claim 7 (original) The method of claim 2 wherein the null frame further includes a destination address field, step (a) further including the step of providing the destination address with a destination address of a corresponding frame received during a receive sequence.

Claim 8 (original) A system for maintaining synchronization in a home network that includes a host Ethernet media access controller and an HPNA chip, wherein control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the system comprising:

(a) means for sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame; and

(b) means for recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs.

Claim 9 (currently amended) ~~The system of claim 8~~ A system for maintaining synchronization in a home network that includes a host Ethernet media access controller and an HPNA chip, wherein control frame and data frame pairs are

transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the system comprising:

(a) means for sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame; and

(b) means for recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs;

wherein the null frame includes a source address field and an Ethernet type field that contains an invalid address.

Claim 10 (original) The system of claim 9 wherein the source address field and the Ethernet type field contain all-zeros.

Claim 11 (original) The system of claim 9 wherein the null frame comprises a minimum size Ethernet frame.

Claim 12 (original) The system of claim 9 wherein the host Ethernet MAC issues a minimum size frame containing a frame control word prior to the data frame during a transmit sequence.

Claim 13 (original) The system of claim 9 wherein the HPNA chip issues a minimum size frame containing a frame status word with the data frame during a receive sequence.

Claim 14 (original) The system of claim 9 wherein the null frame further includes a destination address field that contains a destination address of a corresponding frame received during a receive sequence.

Claim 15 (original) A method for maintaining synchronization in a home network that includes a host Ethernet media access controller program and media interface of an HPNA chip, where control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the method comprising the steps of:

(a) sending a null frame having a source address field and an Ethernet type field from the host Ethernet MAC to the media interface prior to the data frame, wherein the source address field and the Ethernet type field in the null frame include all zeros; and

(b) in response to receiving the null frame by the media interface, recognizing the zeros in the source address field and the Ethernet type field as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs.

Claim 16 (original) The method of claim 15 wherein step (a) further includes the step of providing the null frame as a minimum size Ethernet frame.

Claim 17 (original) The method of claim 16 wherein step (a) further includes the step of issuing from the host Ethernet MAC the null frame containing a frame control word prior to the data frame during a transmit sequence.

Claim 18 (original) The method of claim 17 wherein step (a) further includes the step of issuing from the HPNA chip the null frame containing a frame status word with the data frame during a receive sequence.

Claim 19 (original) The method of claim 18 wherein the null frame further includes a destination address field, step (a) further including the step of providing the destination address with a destination address of a corresponding frame received during a receive sequence.

Claim 20 (original) A home network, comprising:

a host Ethernet media access controller (MAC);

an HPNA chip having a media interface in communication with the host Ethernet MAC; and

control frame and data frame pairs transferred between the host Ethernet MAC and the HPNA chip, wherein the control frame includes a source address field and an Ethernet type field,

wherein synchronicity is maintained between the control frame and data frame pairs by placing an invalid address in the source address field and the Ethernet type field of the control frame, such that the invalid address indicates to a receiver of the control frame that a next received frame will be the data frame.

Claim 21 (original) The system of claim 20 wherein the invalid address comprises all zeros.

Claim 22 (original) The system of claim 20 wherein the null frame comprises a minimum size Ethernet frame.

Claim 23 (original) The system of claim 21 wherein the host Ethernet MAC issues a minimum size frame containing a frame control word prior to the data frame during a transmit sequence.

Claim 24 (original) The system of claim 22 wherein the HPNA chip issues a minimum size frame containing a frame status word with the data frame during a receive sequence.

Claim 25 (original) The system of claim 23 wherein the null frame further includes a destination address field that contains a destination address of a corresponding frame received during a receive sequence.